THE UT/NIST/SA/ISMT THERMOMETRY TEST BED – 2001

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This paper is a sequel to last year's progress report [1] on the development of the Thermometry Test Bed, a joint project by UT (The University of Texas at Austin), NIST (National Institute of Standards and Technology), SA (SensArray Corporation) and ISMT (International SEMATECH). The test bed facility is evolving into a temperature standard, traceable to ITS-90, for commercial sensors targeting applications in RTP and (MO)CVD. The paper highlights key achievements during the past year, including modifications to the facility to accommodate commercial sensors. Results using a standard TC (thermocouple) Instrumented Wafer from SA are presented to characterize the performance of the Test Bed, as well as results from the first set of tests with a SA "sandwich" wafer and with NIST wafers using TFTCs (thin-film thermocouples). The fabrication of hybrid wafers (using both conventional thin wire TCs and TFTCs), which is at the heart of this test bed concept, is on-going and is briefly detailed. Several commercial sensor suppliers are preparing or have initiated tests of their pyrometers. The first pyrometer to be tested is the CI Systems NTM500, and results using this sensor are also reported. The success of this effort continues to be assured by effective interactions of the main players in this project.

INTRODUCTION

The Thermometry Test Bed Project for RTP and (MO)CVD equipment being used in microelectronics manufacturing was conceived and initiated in 1998. At that time, it became clear that the stringent performance specifications for temperature measurement, control, and reproducibility postulated by the IRST (International Roadmap for Semi-Conductor Technology) for the new century (i.e. ± 2 ºC at 1000 ºC, across any wafer, wafer-to-wafer, and at ramp rates up to 400 ºC/sec) continued to be a formidable challenge. It also became apparent that a facility was needed to objectively evaluate and validate the accuracy claims being made with many commercial thermometry systems; i.e. one needed a touchstone for temperature sensors that was traceable to ITS-90 (NIST's International Temperature Standard for 1990). The conceptual design, planning and stepwise realizations of more mature hardware implementations were a joint effort by ISMT and UT, with strong assistance from NIST and SA.

After three years of experimental development, it can be said that the Test Bed is approaching the status of a fully operational and accurate facility for the microelectronics manufacturing industry; i.e for the equipment suppliers and for the IC manufacturers (ISMT member companies). Our RTP2000 paper [1] informed the prospective user community of this unique resource. Modifications made to the Test Bed during the past year include the fabrication of a new bottom flange to allow for easier OEM probe access, upgrades to the data acquisition system for more reliable and versatile data acquisition, and the installation of a new microprocessor-based power controller (Staco Energy Products, Co.). The power controller provides voltage regulation better than 1% for run-to-run repeatability, and has built-in voltmeters and ammeters for precise power measurements.

Figure 1 illustrates the major components of the Test Bed. The top flange assembly is shown in Fig. 1(a). The components visible in Fig. 1(a) are (from the top): the top stainless steel flange, a stack of circular radiation shields, the Boralectric™ ceramic heater (Advanced Ceramics, Inc.), and the rotating diffuser.

The new bottom flange, wafer, and support structure are visible in Fig. 1(b) and Fig. 1(c). The components visible in Fig. 1(b) are (from the top): the SensArray 9-TC Instrumented Wafer, the quartz wafer support (only the front edge is visible), the Inconel support plate (which holds and locates a stack of vertical cylindrical radiation shields, as well as the quartz wafer support), a stack of circular radiation shields (only the edge of the top shield is visible), and the bottom flange. The centering ring assembly around the circumference of the bottom flange is also visible; Viton O-rings in the centering ring assemblies provide the vacuum seal between the top and bottom flanges and the large stainless steel nipple (not shown) that forms the vacuum chamber. Note the polyimide "flat cable" feedthrough used to pass the TC leads from inside the vacuum chamber to the laboratory in the lower right corner of the figure.

In Fig. 1(c), the straight CI lightpipe can be seen emerging from the large feedthrough in the middle of the bottom flange. It passes through small holes drilled in the molybdenum radiation shields and its tip is positioned approximately 1 mm from the underside of the wafer. A large region of the wafer is accessible through this central feedthrough, from its center to its edge on the right-hand side in the figure. The smaller feedthrough directly to the left of the central feedthrough is used for the diffusion pump. The smaller feedthroughs in the foreground are used for other instrumentation or are reserved for future use.

Finally, Fig. 1(d) shows the original bottom flange with an S-shaped CI lightpipe installed. The S-shaped optical probe was needed to accommodate our original bottom flange design, in which the diffusion pump was located in the center of the chamber, directly below the wafer and the instrument feedthroughs were all located around the periphery of the bottom flange. The new bottom flange, as noted above, allows access to the wafer through its center, thus allowing straight lightpipes to be installed and to view any region of the wafer from its center to its edges.

Preparation of trial runs with some of the OEMs (Original Equipment Manufacturers) for commercial pyrometry systems was ramped up during the past year and is expected to be in full swing by the end of 2001. This is occurring concurrently with on-going development and refinement of so-called "hybrid" target wafers, which are instrumented with thin-film and thin-wire thermocouples and which constitute the core embodiment of the temperature standard.

To put it succinctly, the primary objective of the Test Bed project is to provide the industry with an absolute calibration standard for pyrometers that is traceable to ITS-90. This capability will be essential for operating in a "virtual fab" environment (i.e. remote processing) with 300 mm wafers. To fully achieve this objective, several goals had been set after the last RTP meeting to improve the facility as described at that time [1]: i.) Modify

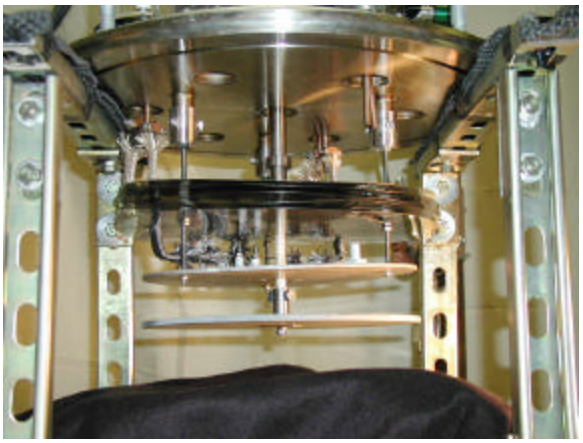

Figure 1(a). Top flange assembly with heater and diffuser

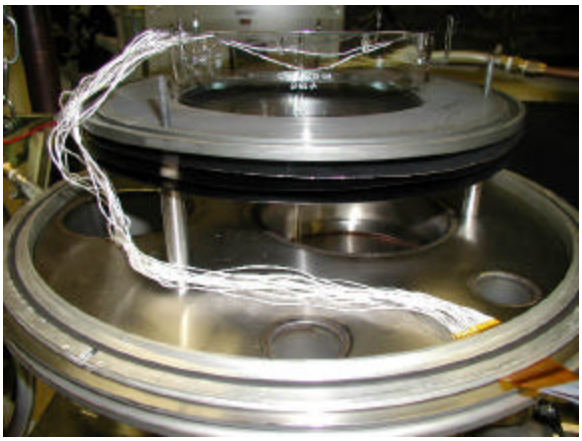

Figure 1(c). Side view showing new bottom flange with straight CI lightpipe installed

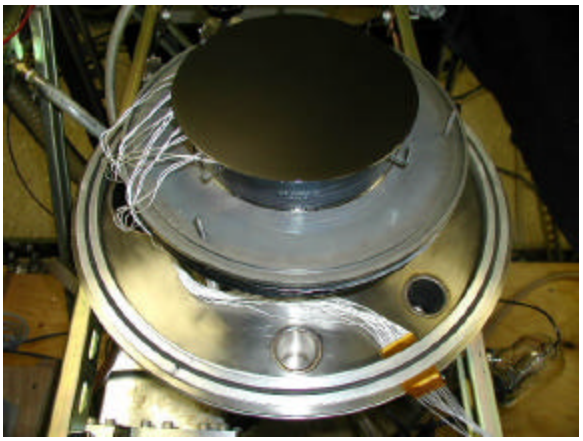

Figure 1(b). Top view of wafer and support structure

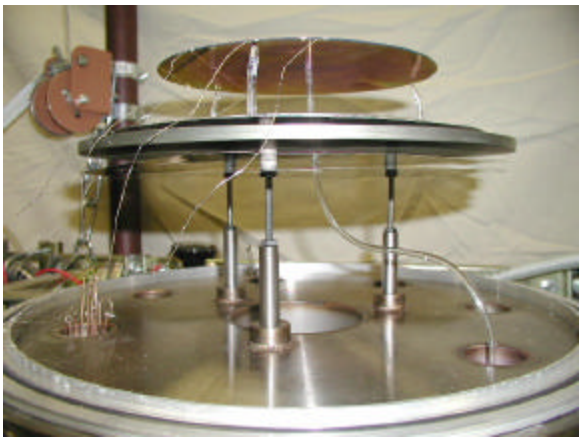

Figure 1(d). Side view showing original bottom flange with S-shaped CI lightpipe installed

the facility to make it fully accessible to various OEM pyrometers, ii.) Optimize the rotating diffuser operation in conjunction with the heater operation to provide the most uniform wafer surface temperature possible, iii.) Fabricate sandwich wafers, TFTC wafers, and "hybrid wafers" combining conventional thin-wire TCs with TFTCs and evaluate their performance as possible temperature standards, and iv.) Initiate collaborations with OEMs.

The first two goals have been largely met, and this paper describes in detail the results associated with them. The third goal has been partially met, with a simple sandwich wafer instrumented with 3 TCs having been made and tested to demonstrate the feasibility of the concept. The development of hybrid wafers is underway. As for the fourth goal, CI Systems has joined this effort and their NTM500 pyrometer has been installed in the Test Bed. Several other OEMs have been identified at this time and are starting hardware preparations.

RESULTS

CI Systems NTM500 Measurements

The CI Systems NTM500 Non-contact Temperature Monitor is a high accuracy and repeatability pyrometer that incorporates real-time same-point emissivity and temperature measurement. The system ends in a fiber bundle and is compatible with a variety of optical interface components. For the Test Bed interface a quartz lightpipe was used - initially a custom designed S shaped rod and later on a straight one. The specified temperature range for RTP applications is 400-1250 ºC, with an accuracy of ±0.8 ºC below 500 ºC and ±0.15%T above 500 ºC.

Figure 2 shows results from our initial test run using the NTM500 system targeting a SensArray TC Instrumented Wafer through the S-shaped optical probe shown in Fig. 1(d) (to accommodate our original bottom flange design, as discussed earlier). For these results, the probe was located within 1 mm of the bottom surface of the standard 11-TC SensArray wafer, between the locations of TC Ch. 7 and TC Ch. 11 (see Table 1 below). Initial calibration of the NTM500 used the Ch. 11 reading. Also, two separate data acquisition systems were used for this test run, due to hardware limitations that will be removed in the future. Thus, a small time lag of a few seconds between the NTM500 measurements and the TC measurements is present. Of course, for measurements made at or near steady-state conditions, this time lag is inconsequential.

To test the performance of the NTM500 system in our Test Bed, a series of arbitrary power adjustments was made to vary the wafer temperature in time. The NTM500 tracked the wafer temperature variations very closely, for this first test run, and with adjustments in alignment of the probe and synchronization of our data acquisition systems, we expect that the agreement between the two will be within the experimental uncertainty of the instruments, which is about 1-2 ºC.

SensArray TC Instrumented Wafer Tests

In order to characterize the behavior of the Test Bed and to demonstrate its ability to provide stable and uniform heating of 200 mm silicon wafers, experiments were conducted using a standard SensArray test wafer instrumented with eleven Type K wire thermocouples embedded at various radial and azimuthal locations. Six TCs (1-6) are located approximately 4 mm from the edge of the wafer, two TCs (7-8) are located approximately 36 mm from the edge, two TCs (9-10) are located approximately 68 mm from the edge, and one TC is located near the center of the wafer (approximately 100 mm from the edge). This is summarized in Table 1, where the various TCs are identified by the Channel number corresponding to their connection to the data acquisition system.

Table 1. Layout of TC Channels on SensArray 11-TC Instrumented Wafer

TC Channel	Distance to edge
1-6	4 mm
7-8	36 mm
9-10	68 mm
11	100 mm

Figures 3(a-c) show the results for a typical experimental run. In Fig. 3(a), data for the full run are shown (Ch. 11 had a faulty connection and no data are shown for this channel). The total temperature variation across the surface of the wafer at any given time is approximately ± 2.5 ºC, which is consistent with other runs using the graphite diffuser. Similar results have been obtained with the other wafers that we have tested in our Test Bed using the graphite diffuser.

After the wafer has reached the steady-state condition, the diffuser is rotated for approximately 10 minute intervals at various speeds. Figures 3(b) and 3(c) show the steady-state results on an expanded scale for diffuser

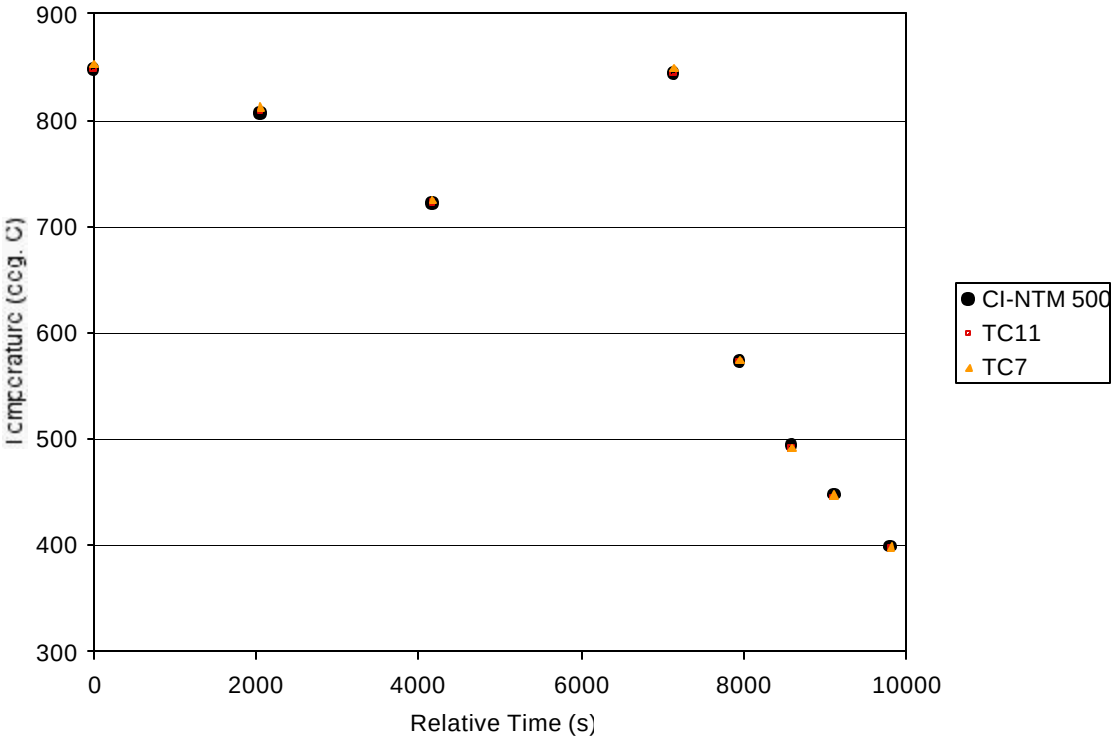

Figure 2. A comparison of NTM500 and SensArray TC temperature measurements with arbitrary heater power adjustments

rotation rates of 30 RPM and 60 RPM, respectively. In general, rotation of the diffuser improves the wafer temperature uniformity by about 1-2 ºC for TCs at the same radial location. More specifically, we typically observe a total temperature variation of about ± 2-3 ºC with no rotation (at fixed radius), which improves to about ± 1 ºC with rotation. This improvement appears to be fairly independent of the rotation rate above about 20 RPM, as observed by comparing Figs. 3(b) and 3(c).

Also shown in the above figures are the measurements taken with the NTM500. Again, the pyrometer tracks well with Ch. 7 (recall that the probe was positioned between Ch. 7 and Ch. 11), even during the periods with large temporal temperature gradients corresponding to the heating and cooling of the wafer. During the steady-state periods shown in Figs. 3(b) and 3(c), the NTM500 measurements agree to within ± 0.5 ºC with the Ch. 7 measurements.

Finally, Fig. 3(d) shows preliminary results from our first experiment using the new bottom flange and straight lightpipe, which was positioned 1 mm below the center of the wafer. For this experiment, a new SensArray TC Instrumented wafer having 9 Type-K TCs was used. In Table 2, the approximate radial locations of the 9 TCs, which are arranged in 4 quadrants, are listed. This experiment also utilized the zirconia diffuser, which is discussed later in the paper. For a given power input to the heaters chosen to result in an average temperature level of approximately 650 ºC, the total variation in temperature at steady-state conditions is ± 1.0 ºC with a diffuser rotation rate of 30 RPM. The measurements from the CI NTM500, using the straight lightpipe, track Ch. 9 (at the center of the wafer) very closely as expected.

The measurements from Ch. 4 and Ch. 8, which are in the same quadrant on the wafer, are

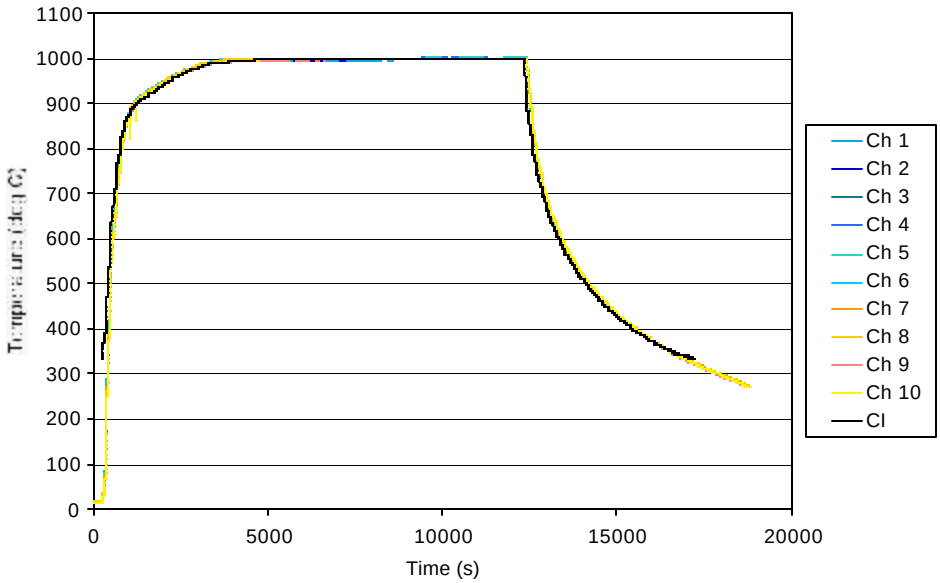

Figure 3(a). Thermal response of SensArray 11-TC Instrumented Wafer (with graphite diffuser)

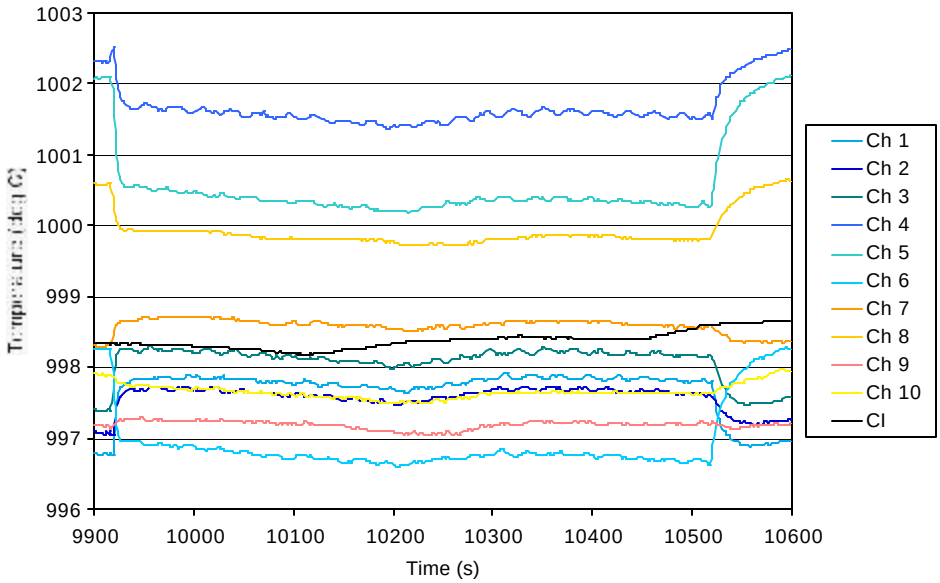

Figure 3(b). Thermal response of SensArray 11-TC Instrumented Wafer (with graphite diffuser) – Expanded scale showing steady-state region with diffuser rotation at 30 RPM

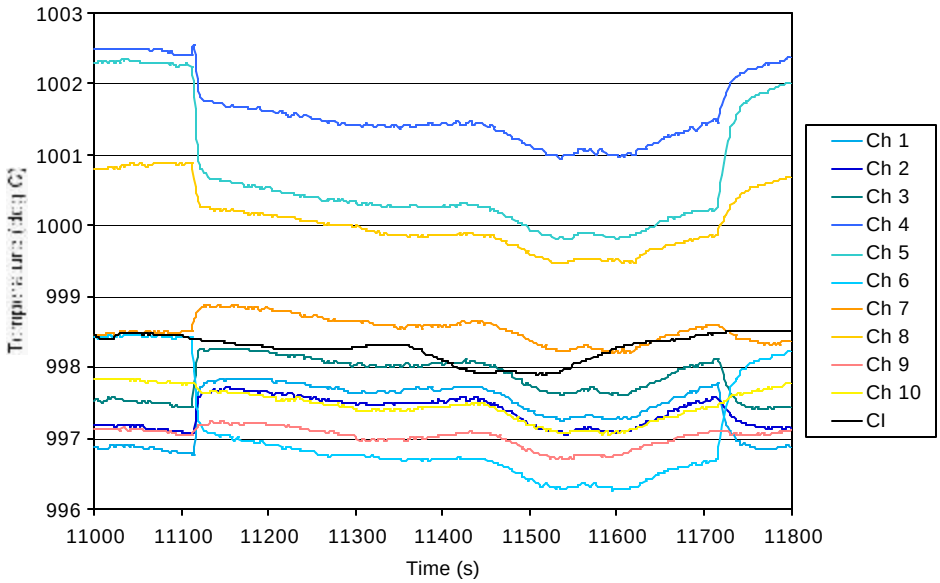

Figure 3(c). Thermal response of SensArray 11-TC Instrumented Wafer (with graphite diffuser) – Expanded scale showing steady-state region with diffuser rotation at 60 RPM

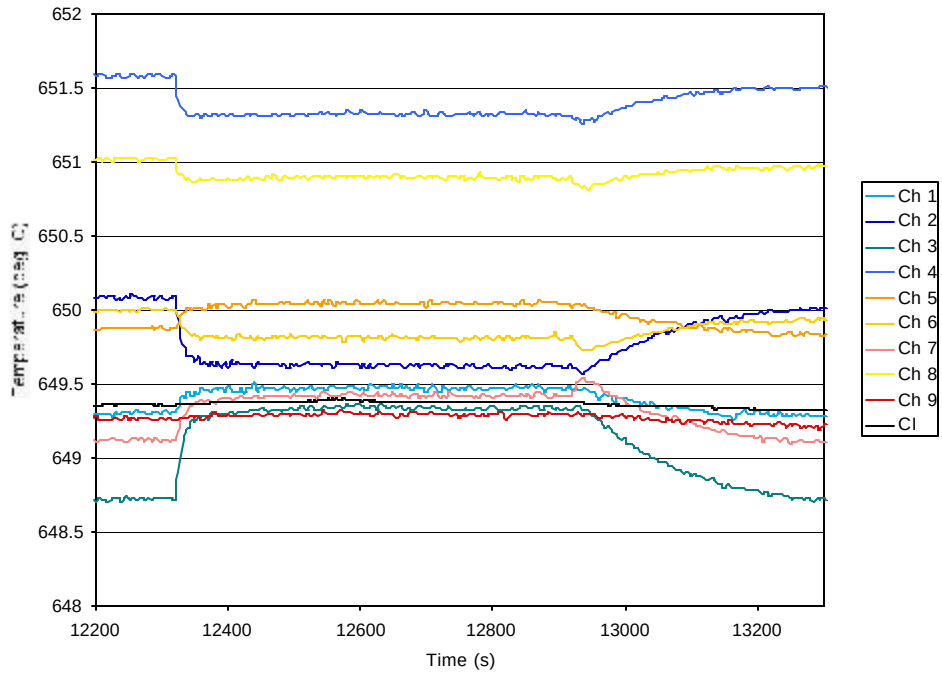

Figure 3(d). Thermal response of SensArray 9-TC Instrumented Wafer (with zirconia diffuser) – Expanded scale showing steady-state region with diffuser rotation at 30 RPM

approximately 1.5 ºC higher than their counterparts in the other 3 quadrants. This could possibly indicate that a small perturbation was present near that quadrant of the wafer. If this were the case and the perturbation were removed, the total variation in temperature as indicated by the other channels would be better than ± 0.5 ºC. Further testing is underway to fully characterize the performance of the new 9-TC wafer in the presence of the straight lightpipe.

Table 2. Layout of TC Channels on SensArray 9-TC Instrumented Wafer

TC Channel	Distance to edge
1-4	5 mm
5-8	50 mm
9	100 mm

NIST 12-TFTC Tests

An important development in RTP temperature measurements and the calibration of radiation thermometers is the use of TFTC instrumented calibration wafers [2]. The use of TFTCs greatly improves the experimental uncertainty of temperature measurements, compared to conventional thin wire TCs, in that conduction losses along the TC circuit are virtually eliminated. TFTC also offer other advantages over traditional wire TCs. A standard uncertainty of 0.3 ºC for differential temperature measurements of up to 10 ºC are reported using TFTCs referenced to Pt/Pd wire TCs, which in turn have a standard uncertainty of 0.1 ºC at 1000 ºC. Kreider et al. [2] and the references cited in that paper provide considerable information about the construction and use of TFTCs for instrumented calibration wafers.

NIST has supplied us with a TFTC-instrumented wafer for testing. The wafer layout provides for redundancy in the temperature measurements, with 12 TC junctions arranged in 4 quadrants at identical radial locations. Thus, if the temperature distribution on the surface of the wafer is axisymmetric, then we will obtain four identical temperature measurements (within experimental uncertainty) at each radial location. Each quadrant of 3 TCs includes a Pt-Pd junction to provide a direct temperature measurement near the edge of the wafer (which is used as a reference for the TFTC measurements), and 2 TFTC junctions (Pt-Rh) to indicate the temperature difference between the reference location and the location of the TF junctions. The two TFTC junctions in each quadrant are at increasing distances from he edge of the wafer (approximately 460 and 840 mm from the wafer edge), while the Pt-Pd TC junction is approximately 5 mm from the edge. Table 3 shows the approximate location of the TC junctions (labeled as "Channels" in Fig. 4).

Table 3. Layout of TC Channels on NIST wafer

Dist. to edge	Quad. 1	Quad. 2	Quad. 3	Quad. 4
460 mm	1	6	7	12
840 mm	2	5	8	11
5 mm	3	4	9	10

Figure 4 shows the voltage measurements obtained from one of our tests using the NIST wafer. Unfortunately, Ch. 1-2 on the wafer were damaged during shipment from NIST to UT, and Ch. 6 opened up during the test due to a broken wire. Thus, no results are provided for those channels. The first figure, Fig. 4(a), shows the temperature response of the wafer with all three heater zones set to the same voltage (50.0 VAC), as it is heated from ambient temperature levels until it reaches the steady-state condition. For this particular test, the graphite diffuser was in place. Power is turned off after approximately 15000 s, and the initial cooling period is also shown. Figure 4(b) is an enlargement of the steady-state period, during which the diffuser is rotated at two speeds, 30 and 60 RPM.

For the Pt-Pd signals (left axes), a reading of 7.6 mV corresponds to approximately 781 ºC, while a reading of 7.7 mV corresponds to

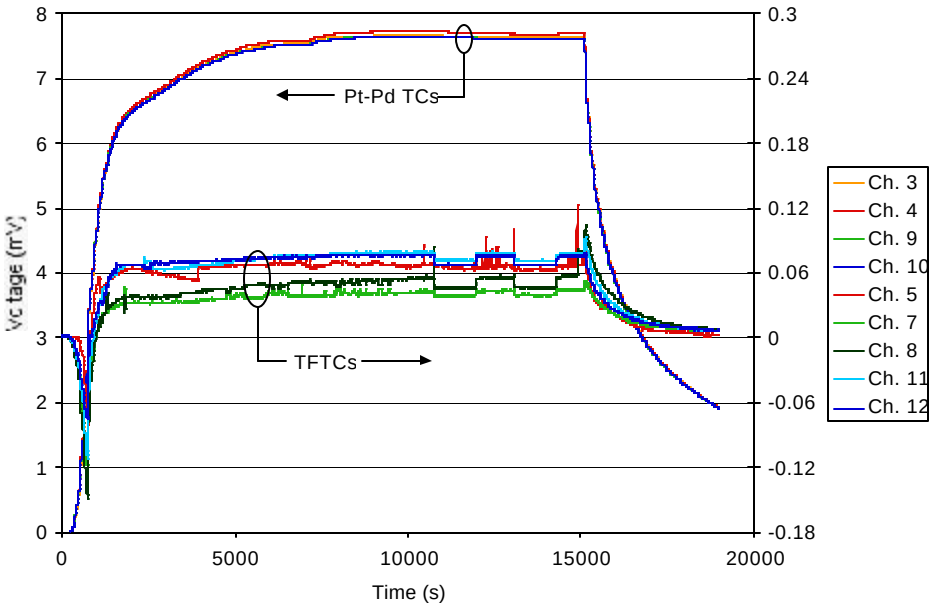

Figure 4(a). Thermal response of NIST TFTC wafer (with graphite diffuser)

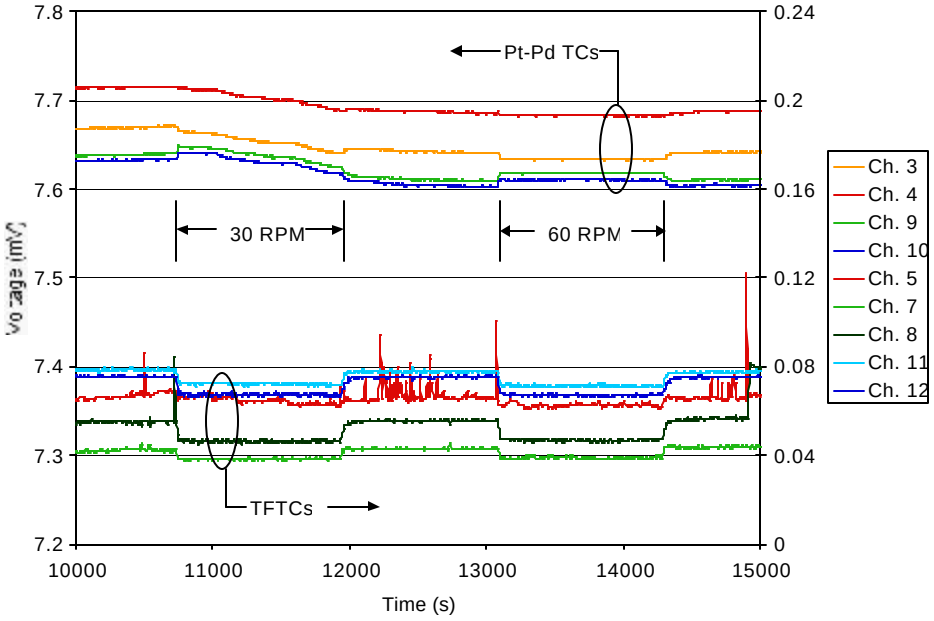

Figure 4(b). Thermal response of NIST TFTC wafer (with graphite diffuser) – Expanded scale showing steady-state region with diffuser rotation

approximately 787 ºC (about 16 µV / ºC). Ch. 3-4 and Ch. 9-10 are in close proximity to each other, with each pair on opposite sides of the wafer The difference in temperature between Ch. 3 and 4 is about 3 ºC; while Ch. 9 and 10 differ by approximately 0.5 ºC. Some variation in temperature readings has been determined through testing to be due to shading from the TC leads. The measurements shown in Fig. 4 are consistent with previous tests using the standard SensArray wafers.

For the TFTC signals (right axes), a reading of 0.04 mV corresponds to a temperature difference of approximately 2.7 ºC, while a reading of 0.08 mV corresponds to a temperature difference of approximately 5.4 ºC (about 14.9 µV / ºC). Thus, the temperature uniformity across the wafer is observed to be within approximately ±2.5 ºC, consistent with previous tests using the graphite diffuser.

Rotation of the diffuser, which should integrate out any non-uniformities due to a non-axisymmetric heat flux from the heater, is observed to result in only a very slight improvement in temperature uniformity. Thus, the (small) differences in temperature at the same radial locations are due to other sources of non-uniformity, such as shading by the TC leads, non-uniform radiative losses from the surfaces of the wafer due to the thin-films and/or weld pads (so-called pattern effects), conduction losses from the wafer supports, etc. Further testing will be necessary to evaluate these various effects and to determine the best possible level of temperature uniformity achievable with the NIST TFTC wafers, but we anticipate that this will be better than ±1.0 ºC.

Rotating Diffuser Tests

The Test Bed has been designed to have a geometrical layout that is as axisymmetric as possible [1]. Even with an axisymmetric geometry, however, non-axisymmetric surface temperature distributions on the test wafers may result due to a non-uniform heat flux originating from the heater. By placing a thin rotating disk, or "diffuser", between the heater and the wafer, an axisymmetric heat flux on the wafer can be achieved. The rotating diffuser absorbs thermal energy from the heater on its top side. This energy is then conducted through the thickness of the diffuser to its bottom side, where it is then re-radiated to the wafer. Rotation of the diffuser integrates out any non-uniformities in heat flux originating from the heater. Since such non-uniformities are inherent in most heater designs, the installation of a rotating diffuser can lead to considerable improvements in temperature uniformity on the surface of the wafer.

Earlier tests using relatively thick diffusers made of graphite foam and silicon carbide confirmed that a high level of axisymmetry could be achieved for the wafer temperature distributions. However, little control over the radial temperature distribution was possible, despite the heater having three separate zones in the radial direction (an inner zone, a middle zone, and an outer zone). Due to increased heat losses from the edge of the wafer, a radial temperature gradient was always present, with the highest temperature levels occurring at the middle of the wafer. Even if no power were supplied to the inner heater zone and all of the power were supplied to the outer zone, the radial gradient persisted (although a slight improvement was noted). The best result obtainable was an overall temperature uniformity of about ±2.5 ºC (or ±1.0 ºC at any given radial location).

The reason for the lack of radial control was assumed to be due to the relatively low thermal resistance imposed by the diffuser, which used materials having relatively high thermal conductivities and which were relatively thick. Thus, the non-uniform heat flux imposed in the radial direction by supplying more power to the outer heater zone than the inner zones was effectively being smeared out by diffusion. In order to preserve an imposed radial distribution of the heat flux, the rotating diffuser should present a high resistance to thermal diffusion. Thus, it was hypothesized that using a thin diffuser made of relatively low thermal conductivity material would result in more uniform radial temperature distributions when the outer zone of the heater was supplied with more power than the inner zones.

Five different rotating diffuser materials were tested, to determine which allows for the greatest radial temperature uniformity. The materials tested were: graphite foam (Poco Graphite, Inc.), zirconia, alumina, silicon carbide, and mullite. Zirconia, alumina, and mullite are considered to be low thermal conductivity materials.

As expected, the zirconia diffuser (lowest k) appears to best preserve the imposed radial heat flux distribution. Additional tests to determine the highest possible level of temperature uniformity using the zirconia diffuser were conducted, and the best results obtained to date are shown in Fig. 5.

In Fig. 5, the TCs corresponding to Ch. 1-5 are close to the edge of the wafer, Ch. 7-10 are in the interior of the wafer, and Ch. 11 is at the center of the wafer (see Table 1). The overall temperature uniformity is better than ±1.5 ºC, which is approaching the experimental uncertainty of the measurements.

FABRICATION OF HYBRID TARGET WAFERS

As stated in last year's project description [1], special target wafers are to be fabricated for the test bed, and will contain dual sets of thermocouples, i.e. wire TCs embedded in the wafer and TFTCs installed on one surface of the wafer. The wire TC and TFTC junctions are to be co-located (in wafer polar coordinates) so that any point on the wafer being targeted by a pyrometer presents a pair of TC readings (giving some indication of thermal gradients through the wafer thickness). This concept for the target wafer is shown schematically in Fig. 2 of Ref. [1].

Actual fabrication of such wafers will be based on using a "sandwich" assembly for placement of the wire TCs. This notion is illustrated in Fig. 6 for just one wire TC and one TFTC, for clarity. The half of the sandwich to receive wire TCs has precision grooves cut into one side, which are laid out to permit later placement of the junctions at predetermined locations. This grooved half is subsequently

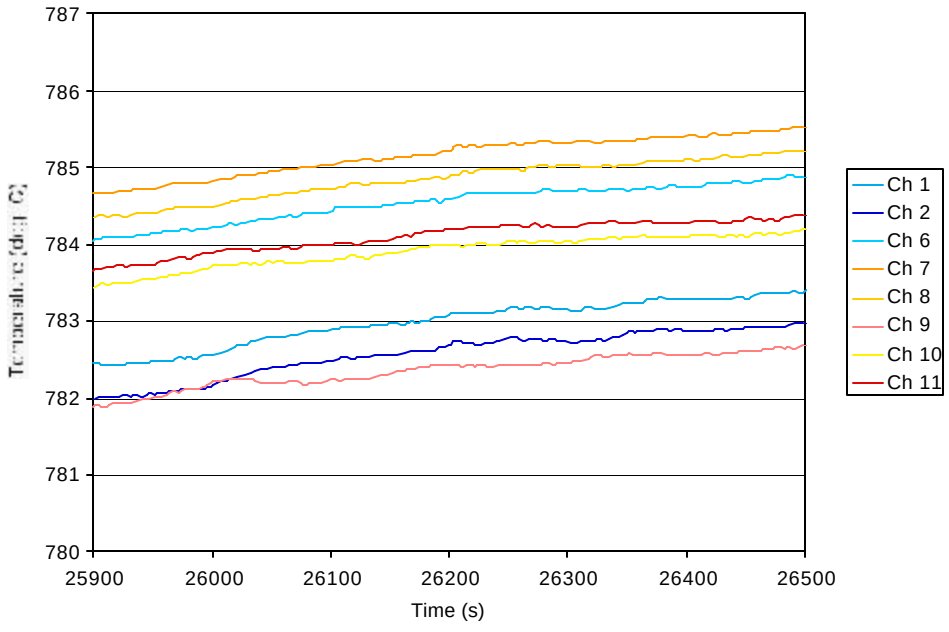

Figure 5. Thermal response of SensArray TC-instrumented wafer (with zirconia diffuser) – Expanded scale showing temperature distribution as the steady-state condition is approached

matched and bonded to a second (ungrooved) half that serves as a cover plate for the grooves, thus transforming them into closed channels for later installation of the wire TCs. (Note that presently both halves are supplied with standard wafer thickness, resulting in a double-thick sandwich assembly.)

To assure a pristine bonding interface, all wafers are initially (before the groove cutting) supplied with a protective oxi-nitride coating. This is removed by etching immediately prior to bonding. Details of the bonding operation depend on the supplier. In our case, two suppliers are being used: the Silicon Genesis Corporation and the Fraunhofer Institute for Reliability and Micro-Integration at the University of Chemnitz, Germany. More than one supplier was deemed necessary in this crucial step to provide an enhanced data base with respect to quality and durability of bonding. After successful bonding, a fresh thermal oxide layer is applied to each sandwich assembly. This serves as a "base coat" for the deposition of TFTCs at NIST.

After these metallizations have been applied (however as yet without terminations), the sandwich assemblies return to SA for insertion of the wire TCs. Each TC wire is threaded into a protective quartz capillary before insertion into the open conduits provided by the bonding operation. After appropriate terminations for the wire leads have been installed along the wafer edge, the sandwich assembly finally returns to NIST for installation of terminal posts along the edge, pigtails to the Pt weld pads, external wire leads and final anneal followed by calibration.

Needless to say, the above fabrication sequence involves many delicate operations, requiring innovative tooling and methodology. Therefore, it was decided to initially pursue the learning curves for sandwich wafers with wire TCs and for deposition of TFTCs separately.

The first sandwich wafer to be delivered for testing included 3 wire TC junctions at different radial locations across the wafer. The results of our initial test of this wafer are shown in Fig. 7. One of the TCs, Ch. 1, was damaged at some point prior to its installation and never produced a signal. The signal from Ch. 2 was typical of the signals from any of the channels on the standard SensArray TC instrumented wafer, and the NTM500 probe tracked Ch. 2 very closely. However, the signal from Ch. 3 exhibited intermittent spikes at elevated temperatures, indicating a possibly imperfect TC junction, although the source of the spikes has not been determined. The difficulties with Ch. 1 and Ch. 3 suggest that further improvements need to be made for the fabrication, insertion, and use of the TCs.

The results from Ch. 2 indicate that the thermal response of the sandwich wafer is not appreciably different than that of other test wafers. The peak temperatures were slightly higher for the same power settings (1006 ºC compared to 1002 ºC with a standard SensArray wafer), due to the increased thickness of the sandwich wafer and/or different thermophysical properties. The pyrometer tracked the temperature variation with a more-or-less constant bias of about 5 ºC (note that it was not re-calibrated for the sandwich wafer, and that the probe location was offset from Ch. 2 and Ch. 3). The rotating diffuser did not seem to have any noticeable effect on the TC signals, possibly due to the increased thickness of the wafer or increased thermal resistances. The TC signals exhibited a slight high-frequency noise component, which might be another indication of imperfect TC junctions. Given these results, though, we believe that the concept of developing hybrid wafers as described above is worth pursuing.

Concurrently with the development of the sandwich wafers, fabrication of several trial lots of "simple" hybrid wafers (with only four wire TCs and four co-located TFTCs) was begun. Unfortunately, the majority of grooved wafers fractured, along grooves, during transport to the bonding operations. This kind of yield loss had not been experienced before and replacement lots are now under way, using an improved "shock proof" type of packaging for all transfers after the groove cutting.

Cut-Away Phantom View of "Hybrid" TC Wafer Showing Co-location of Thin-Film and Thin-Wire Junctions

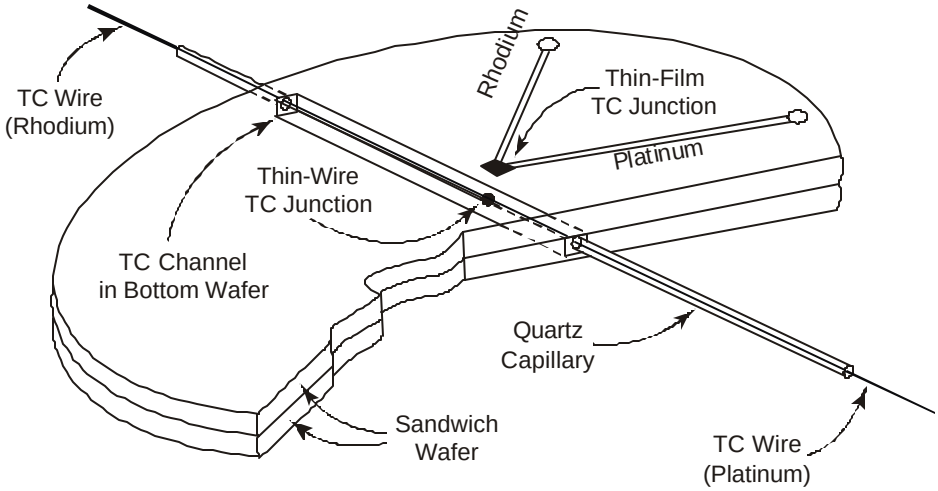

Figure 6. Development hybrid of test wafers

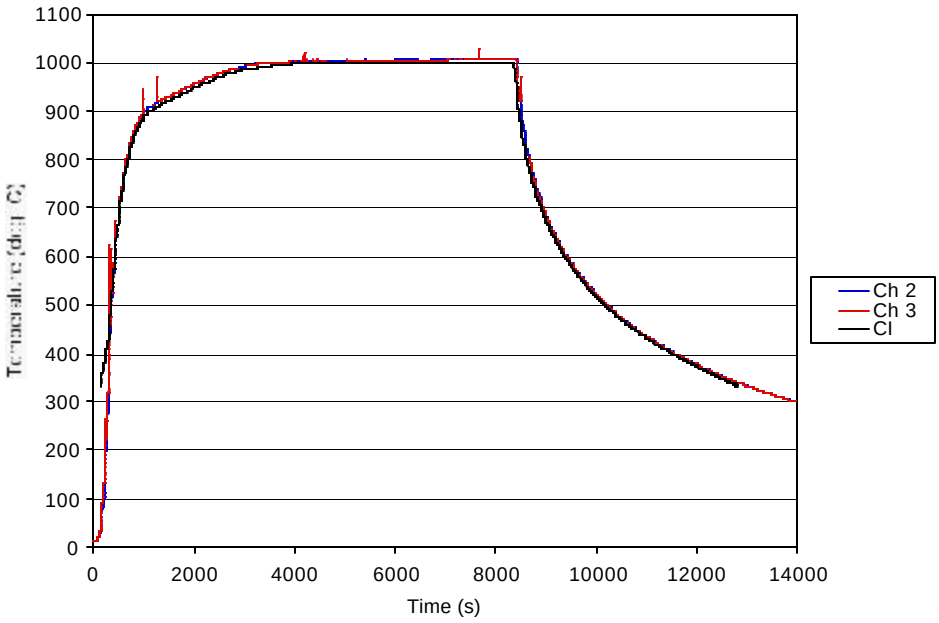

Figure 7. Thermal response of Sandwich wafer with 3 wire TCs

SUMMARY

Further improvements have been made to the Thermometry Test Bed since our last report, to ensure uniform wafer heating, system stability, and versatility. The performance of the Test Bed is indicated by the following characteristics:

i.) Run-to-run repeatability better than ± 1.0 ºC at 1000 ºC,

ii.) Overall temperature uniformity better than ± 1.5 ºC (better than ± 1.0 ºC at any given radial location).

While a formal analysis of the experimental uncertainty of the measurements has not been performed, these values are believed to be comparable to the experimental uncertainty and further improvements are not likely. However, these values exceed the design requirements of the Test Bed and thus are sufficient to satisfy the larger objectives of this project.

Modifications have been made to the bottom flange, allowing various OEM pyrometers to be accommodated. Initial testing of the CI Systems NTM500 sensor has been completed, and the measurements agree with the TC readings to within ± 1.0 ºC. We will continue to test various OEM probes as they become available.

Finally, we have performed tests using a number of different instrumented test wafers, all of which yield similar results. In particular, the NIST 12-TFTC wafer performance is comparable to the standard SensArray wafer performance. Unfortunately, only a limited amount of data could be obtained from the first sandwich wafer, but it too appeared to be consistent with the other wafers. We will evaluate the hybrid test wafers incorporating both thin-film thermocouples and thin-wire thermocouples as they become available.

ACKNOWLEDGMENTS

We wish to thank the following organizations and their staff for their diligence, good will, and perseverance as partners in the Test Bed Project: NIST for their innovative work with TFTC technologies; SA for groove cutting and TC installation; the UT Mechanical Engineering shop for innovative hardware implementations of the Test Bed; the ISMT ATDF (Advanced Technology Development Facility) for preparing, handling, and shipping special wafer products; Silicon Genesis Corporation and the Micro-Integration Laboratory at the University of Chemnitz for their very important wafer bonding know-how, and CI-Semi / CI-Systems for their NTM500 pyrometry system. The efforts of K. G. Kreider at NIST to supply us with TFTC-instrumented wafers, and of management at CI-Semi to release a NTM500 system for use in the Test Bed, are particularly appreciated. The UT members of this project would also like to acknowledge the support of the staff and management of International SEMATECH.

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